Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit for aggregating a plurality of input data streams from first processors into one data stream for a second processor, said circuit comprising:

a plurality of ingress data ports, each said ingress data port coupled to a corresponding first processor and adapted to receive an input data stream from the corresponding first processor, each input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;

an aggregation module coupled to said plurality of ingress data ports and configured to receive the plurality of input data streams from the first processors using the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor, said aggregation module adapted to analyze and combine the plurality of input data streams into one aggregated data stream in response to the priority factors and to generate a packet descriptor comprising a reference to a memory location of its analyzed data packet;

a memory coupled to said aggregation module, said memory adapted to store analyzed data packets; ~~and~~

said memory comprising a plurality of priority queues each provided for a corresponding priority class, adapted to store the packet descriptor of each of the analyzed data packets classified to the corresponding priority class, the packet descriptor containing a reference to the memory location of its analyzed data packet in said memory; and

an output data port coupled to said aggregation module, said output data port adapted to output the aggregated data stream to the second processor.

2. (Original) The circuit of claim 1, wherein each of the first processors and the second processor transmits and receives a data stream through a logical interface providing logical interconnection between a Media Access Control sublayer (MAC) and a Physical layer (PHY).

3. (Original) The circuit of claim 1, wherein the first processors are Layer-2 switching processors.

4. (Original) The circuit of claim 1, wherein the second processor is a data packet processor.

5. (Original) The circuit of claim 1, wherein said memory is an external buffer memory.

6. (Original) The circuit of claim 1, further comprising:

an egress data input port adapted to receive a data stream from the second processor, the data stream formed of egress data packets;

a plurality of egress data output ports, each adapted to output an output data stream to a corresponding one of the first processors; and

a forwarding module coupled between said egress data input port and said egress data output port, said forwarding module adapted to forward an egress data packet in the data stream from the second processor to one of the egress data output port in response to destination information associated with said egress data packet.

7. (Currently Amended) The circuit of claim 1, wherein:

said ingress data ports include a first data port for receiving a first input data stream and a second data port for receiving a second input data stream; and

said aggregation module includes:

a first packet analyzer coupled to said first data port, adapted to classify each of the ingress data packets in the first data stream into one of predetermined priority classes based on the priority factors;

a second packet analyzer coupled to said second data port, adapted to classify each of the ingress data packets in the second data stream into one of predetermined priority classes based on the priority factors;

a queue module having

~~a plurality of priority queues each provided for the corresponding priority class, adapted to store a packet descriptor of each of the analyzed data packets classified to the corresponding priority class, the packet descriptor containing a reference to a memory location of its analyzed data packet in said memory, and~~

a selection logic implementing a queue scheme, adapted to arbitrate and select a packet descriptor from among the priority queues;

a first write interface coupled to said first packet analyzer, adapted to write the analyzed data packets into said memory at the memory location indicated by the corresponding packet descriptor;

a second write interface coupled to said second packet analyzer, adapted to write the analyzed data packets into said memory at the memory location indicated by the corresponding packet descriptor;

a common read interface coupled to said queue selection logic, adapted to read a data packet corresponding to the selected packet descriptor from said memory; and

an output module to send the data packets read from said memory to said output data port as the aggregated data stream.

8. (Original) The circuit of claim 7, wherein:

said first packet analyzer includes a first data decoder coupled to said first ingress data port, adapted to decode a header of each ingress data packet to extract the priority factors; and

said second packet analyzer includes a second data decoder coupled to said second ingress data port, adapted to decode a header of each ingress data packet to extract the priority factors.

9. (Original) The circuit of claim 7, wherein said output module comprises:

a read buffer coupled to said common read interface.

10. (Original) The circuit of claim 9, wherein said output module further comprising:

a data encoder coupled to said read buffer, adapted to encode the data packets into an interface format corresponding to the first interfaces before sending from the output data port.

11. (Original) The circuit of claim 7, wherein said aggregation module further comprises:

a first write buffer coupled between said first packet analyzer and said first write interface; and

a second write buffer coupled between said second packet analyzer and said second write interface.

12. (Original) The circuit of claim 11, wherein said aggregation module further comprises:

a flow control module adapted to assert a flow control signal if an amount of data stored in said first or second write buffer exceeds a threshold.

13. (Original) The circuit of claim 7, further comprising:

a flow control module adapted to assert a flow control signal if an amount of data stored in a corresponding priority queue in said queue module exceeds a threshold.

14. (Original) The circuit of claim 7, further comprising:

an egress data input port adapted to receive a data stream from the second processor, the data stream formed of egress data packets;

a plurality of egress data output ports, each adapted to output an output data stream to a corresponding one of the first processors;

a forwarding module coupled between said egress data input port and said egress data output ports, said forwarding module adapted to forward an egress data packet in the data

stream from the second processor to one of the egress data output port in response to destination information associated with each egress data packet.

15. (Original) The circuit of claim 14, wherein said aggregation module further comprises:

a flow control module adapted to assert a flow control signal if an amount of data stored in said first or second write buffer exceeds a threshold, or if an amount of data stored in a corresponding priority queue in said queue module exceeds a threshold.

16. (Original) The circuit of claim 15, wherein said flow control module sends the flow control signal to said second processor, said second processor insert a pause control packet for said first processors in the data stream.

17. (Previously Presented) The circuit of claim 1:

wherein the aggregation module is implemented by a programmable device.

18. (Previously Presented) The circuit of claim 1:

wherein the priority factors include an indication of whether the ingress packet contains protocol data or not.

19. (Previously Presented) The circuit of claim 18, wherein the priority factors further include:

per-port priority; and

virtual LAN priority.

20. (Previously Presented) A circuit for aggregating an input data stream from a first processor into an aggregated data stream for a second processor, said circuit comprising:

a first data link adapted to receive the input data stream from the first processor, the first data link having a first bandwidth, the input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;

an aggregation module coupled to the first data link and adapted to receive the input data stream from the first processor via the first data link, said aggregation module adapted to analyze and selectively recombine the ingress data packets in response to the priority factors so as to generate an aggregated data;

a memory coupled to said aggregation module, said memory adapted to store analyzed data packets; and

a second data link coupled to said aggregation module, the second data link having a second bandwidth smaller than the first bandwidth, said second data link adapted to output the aggregated data stream from the aggregation module to the second processor.

21. (Original) The circuit of claim 20, wherein the first processor and the second processor include an interface providing logical interconnection between a Media Access Control sublayer (MAC) and a Physical layer (PHY).

22. (Original) The circuit of claim 20, wherein said memory is an external buffer memory.

23. (Previously Presented) The circuit of claim 20, wherein said aggregation module comprising:

a packet analyzer adapted to classify each of the ingress data packets into one of predetermined priority classes based on the priority factors;

a queue module comprising

a plurality of priority queues each provided for the corresponding priority class, adapted to store a packet descriptor of each of the analyzed data packets classified to the corresponding priority class, the packet descriptor containing a reference to a memory location of its analyzed data packet in said memory, and

a selection logic implementing a queue scheme, adapted to arbitrate and select a packet descriptor from among the priority queues;

a read interface coupled to said queue module, adapted to read a data packet corresponding to the selected packet descriptor from said memory; and

an output module to send the data packets read from said memory to the second data link as the aggregated data stream.

24. (Previously Presented) The circuit of claim 23, wherein said packet analyzer comprises:

a data decoder coupled to the first data link, adapted to decode a header of each ingress data packet to extract the priority factors.

25. (Original) The circuit of claim 23, wherein said output module comprises:

a read buffer coupled to said read interface.

26. (Previously Presented) The circuit of claim 25, wherein said output module further comprises:

a data encoder coupled to said read buffer, adapted to encode the data packets before sending using the second data link.

27. (Original) The circuit of claim 23, wherein said aggregation module further comprises:

a write interface coupled to said packet analyzer, adapted to write the analyzed data packets into said memory at the memory location indicated by the corresponding packet descriptor.

28. (Original) The circuit of claim 27, further comprising:

a write buffer coupled between said packet analyzer and said write interface.

29. (Original) The circuit of claim 28, further comprising:

a flow control module adapted to assert a flow control signal if an amount of data stored in said write buffer exceeds a threshold.

30. (Original) The circuit of claim 23, further comprising:

a flow control module adapted to assert a flow control signal if an amount of data stored in a corresponding priority queue in said queue module exceeds a threshold.

31. (Canceled)

32. (Previously Presented) A method for aggregating a plurality of input data streams from first processors into one data stream for a second processor, said method comprising:

receiving an input data stream from each of the first processors, each input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;

analyzing and classifying each of the ingress data packets into one of predetermined priority classes based on the priority factors;

storing an analyzed data packet in a memory;

generating a packet descriptor for the analyzed ingress data packet, the packet descriptor containing a reference to a memory location of its analyzed data packet stored in the memory;

placing the packet descriptor in a priority queue corresponding to the priority class of the data packet;

arbitrating and selecting a packet descriptor from among the priority queues using selection logic implementing a queue scheme;

reading a data packet corresponding to the selected packet descriptor from the memory; and

sending the data packets read from the memory to the second processor as an aggregated data stream.

33. (Original) The method of claim 32, wherein said analyzing comprises:

decoding a header of each ingress data packet to extract the priority factors.

34. (Original) The method of claim 32, further comprising:

buffering the analyzed data packet in a write buffer before storing in the memory.

35. (Original) The method of claim 34, further comprising:

asserting a flow control signal if an amount of data stored in the write buffer exceeds a threshold.

36. (Original) The method of claim 32, further comprising:

buffering the data packet read from the memory in a read buffer.

37. (Original) The method of claim 32, further comprising:

encoding the data packets into an interface format before sending to the second processor.

38. (Original) The method of claim 32, further comprising:

asserting a flow control signal if a length of a corresponding priority queue exceeds a threshold.

39. (Original) The method of claim 32, wherein said memory is an external buffer memory.

40. (Original) The method of claim 32, wherein each of the first processors and the second processor transmits and receives a data stream through a logical interface providing logical interconnection between a Media Access Control sublayer (MAC) and a Physical layer (PHY).

41. (Original) The method of claim 32, wherein said analyzing and classifying, said generating, and said storing are performed separately for each data stream.

42. (Original) The method of claim 32, wherein, in said placing, the packet descriptors from each data stream of a same priority class are placed in the same priority queue for that priority class.

43. (Original) The method of claim 32, wherein said arbitrating and selecting, said reading, and said sending are performed as a single data channel.

44. (Original) The method of claim 32, wherein said analyzing and classifying comprises:

protocol-filtering to determine if the ingress data packet is a certain protocol packet.

45. (Original) The method of claim 44, wherein the priority factors comprise:

protocol filter priority;

per-port priority; and

virtual LAN priority.

46. (Currently Amended) A method for aggregating a plurality of input data streams from first processors into one data stream for a second processor, said method comprising:

providing, for each first processor, an analyzer corresponding to the first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor;

receiving an input data stream from each of the first processors, each input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;

generating an aggregated data stream by combining the plurality of input data streams into one aggregated data stream in response to the priority factors, the priority factors including an indication of whether the ingress packet contains protocol data or not, wherein the generating comprises, for each first processor, receiving the input data stream from the first processor at an analyzer corresponding to the first processor, and analyzing the input data stream received from the first processor using the analyzer to classify each of the ingress data packets into one of a plurality of priority classes based on the priority factors included in the ingress data packet; and

outputting the aggregated data stream to the second processor.

47. (Previously Presented) A method for aggregating data packets, said method comprising:

receiving an input data stream from a first processor via a first data link having a first bandwidth, the input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;

generating an aggregated data stream by analyzing and selectively recombining the ingress data packets in response to the priority factors, the priority factors including an indication of whether the ingress packet contains protocol data or not; and

outputting the aggregated data stream to a second processor via a second data link having a second bandwidth, wherein the first bandwidth is greater than the second bandwidth.

48 - 70. (Canceled)